REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, each of independent claims 1, 2, 4, 5, 9, 10, 15, 41, 43 and 45-47 has been amended to recite that the chemically mechanically polished surface is formed on the oxidation prevention film on the circuit formation surface and on the (buried) insulating film over the trench; similarly, claim 54 has been amended to recite that after burying the buried insulating film, the insulating film is removed on the oxidation prevention film on the circuit formation surface and on the buried insulating film over the trench.

It is respectfully submitted that the amendments to the independent claims as set forth in the foregoing is clearly supported by the original disclosure of the above-identified application, and do not constitute new matter within the meaning of 35 USC §132. Thus, note steps (6) and (7) on page 7 of Applicants' specification, with the headings respectively of "Step to remove buried insulating film formed on oxidation prevention film" and "Step to oxidize semiconductor substrate after removal of buried insulating film formed on oxidation prevention film". Note also, for example, Figs. 6G and 6H of Applicants' original disclosure, together with the descriptions from page 22, line 13 through page 23, line 19, of Applicants' specification. Clearly, as seen in various figures in Fig. 6(noting especially Figs. 6G and 6H), the buried insulating film 9 is removed (for example, by chemical mechanical polishing) both over the oxidation prevention film on the circuit formation surface and on the buried insulating film over the trench. Note also, for example, Fig. 2K, obtained by carrying out chemical

mechanical polishing on Fig. 2G, it being disclosed that the thickness of the oxidization prevention film 17 in Fig. 2G is thinner than in Fig. 2K. From this fact, and noting that the oxidation prevention film is used as an etching stopper, clearly the etched surface is formed on the buried oxidation film and the oxidation prevention film on the circuit formation surface.

Initially, it is respectfully requested that the present amendments be entered, notwithstanding Finality of the Office Action mailed June 1, 2004. It is respectfully submitted that the present amendments clarify recitations previously in claims of the above-identified application, based upon supporting arguments previously made. Thus, it is respectfully submitted that the present amendments do not raise any new issues. As set forth previously, it is respectfully submitted that the present amendments do not raise any issue of new matter. Furthermore, by further clarifying recitations in the present claims consistent with arguments made in the above-identified application, it is respectfully submitted that the present amendments materially limit issues remaining in the above-identified application; and, at the very least, present the claims in better form for appeal. Moreover, noting additional contentions and new grounds of rejection in the Office Action mailed June 1, 2004, it is respectfully submitted that the present amendments are clearly timely.

In view of the foregoing, it is respectfully submitted that Applicants have made the necessary showing under 37 CFR § 1.116(c); and that, accordingly, entry of the present amendments is clearly proper.

Applicants respectfully note the objection to claims 64 and 65, in that both claims depend on claim 45 and recite the same limitation. Claim 65 has been amended to be dependent on claim 46; accordingly, the basis for the objection to claims 64 and 65 is moot.

Applicants respectfully traverse the objection to the Amendment filed March 23, 2004, under 35 USC §132, and the rejection of claims 55-66 under the first paragraph of 35 USC §112, as failing to comply with the written description requirement, as set forth in Items 2 and 3 on pages 2 and 3 of the Office Action mailed June 1, 2004. Contrary to the conclusion by the Examiner, it is respectfully submitted that there is clear support in Applicants' original disclosure for the recitation in claim 55-66 that the chemically mechanically polished surface is formed over the circuit formation surface and over the trench, and wherein in performing the selective thermal oxidation, the semiconductor substrate having the chemically mechanically polished surface formed over the circuit formation region and over the trench is selectively thermally oxidized; and that claims 55-66 do not introduce new matter into the disclosure. Thus, attention is respectfully directed to page 7, lines 8-15 of Applicants' specification, describing a "Step to remove buried insulating film formed on oxidation prevention film", with the description that the buried insulating film is etched back by chemical-mechanical polishing or dry etching. Page 7, lines 16-24 recite the subsequent step of oxidizing the semiconductor substrate after removal of buried insulating film formed on the oxidation prevention film. Clearly, Applicants' original disclosure shows that it was within the contemplation of the inventors that their invention included chemical-mechanical

polishing of the buried insulating film formed on the oxidation prevention film, with a subsequent oxidation of the substrate (which is a selective oxidation).

In addition, attention is respectfully directed to, for example, Figs. 2G and 2H of Applicants' original disclosure, together with the description in connection therewith on pages 13 and 14 of Applicants' original disclosure; and, for example, Figs. 6G and 6H, together with the description on pages 22 and 23 of Applicants' original disclosure. Clearly, as can be seen in the drawing figures, the insulating film 9 is removed over the oxidation prevention (silicon nitride) film 17 on the circuit formation surface, as well as over the trench. Thus, clearly there is support in Applicants' original disclosure for recitation of formation of the chemically mechanically polished surface over the circuit formation surface and over the trenches, and with respect to the selective thermal oxidation, in claims 56-65.

The contention by the Examiner in Item 9 on page 21 of the Office Action mailed June 1, 2004, that Applicants' disclosure specifically states that the additional oxidation may be executed before the chemical mechanical polishing or after the step (8) of removing the oxidation prevention film formed on the circuit formation surface of the semiconductor substrate, is noted. However, Applicants' disclosure also discloses that the additional oxidation may be executed after the chemical mechanical polishing and before removal of the oxidation prevention film. Note step (7), between steps (6) and (8), on pages 7 and 8 of Applicants' specification. It is respectfully submitted that one feature of the present invention is the sequencing of processing as in the present

claims. Thus, Applicants' specification clearly supports the presently claimed processing, within the description requirement of the first paragraph of 35 USC §112.

While there are various embodiments of the present invention in Applicants' disclosure, including that in the present claims, this does not support the contention by the Examiner that the presently claimed subject matter is not described within the requirements of the first paragraph of 35 USC §112.

The Examiner has pointed to various statements in Applicants' specification where thermal oxidation is again carried out before etching the buried insulating film 9. This is a description of an additional feature of the present invention, and provides no support whatsoever for a conclusion that the presently claimed invention is not described in the specification of the above-identified application, within the requirements of the first paragraph of 35 USC §112.

The requirement by the Examiner for removal of new matter in new claims 55-66 is noted. As clearly established in the foregoing, the present claims 55-66 do not include new matter, so that there is no need for removal of any matter therefrom.

The additional contention by the Examiner in Item 9 on page 21 of the Office Action mailed June 1, 2004, that Applicants "fail to point out the specific portion of the original written disclosure" directed to what the Examiner contends to be new matter, e.g., additional oxidation is performed on the CMP surface, is respectfully traversed. Applicants have set forth clearly in the foregoing, as well as in prior amendments, specific support in the original written disclosure for recitations in the present claims. Clearly, the Examiner errs in his conclusion concerning new matter.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed June 1, 2004, that is, the teachings of the U.S. patents to Mehta, et al., No. 5,646,063, and to Otsu, No. 5,236,861, and European Patent Application No. 459,397 (which the Examiner has referred to as "Takahashi"), under the provisions of 35 USC §103.

It is respectfully submitted that the references as applied by the Examiner would have neither taught nor would have suggested such a method for fabricating a semiconductor device or semiconductor substrate as in the present claims, including, after forming a trench (trenches) or trench region, thermally oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench, so as to form, e.g., a first curvature of the upper end portion of the trench; and after burying a buried insulating film into the trench and on an oxidation prevention film on a substrate having the trench formed therein, removing the insulating film by chemical mechanical polishing to form a chemically mechanically polished surface on the oxidation prevention film on the circuit formation surface and on the buried insulating film over the trench, and thereafter performing selective thermal oxidation of the substrate after having formed this chemically mechanically polished surface, so as to thermally oxidize only a portion of the substrate, at the upper end portion of the trench, and not substantially at other portions of the substrate lining the trench, so as to increase a curvature of the upper end portion of the trench substantially without oxidizing the other portions of the semiconductor substrate lining the trench. See claim 1. Note also

claims 2, 4, 5, 9, 10 and 15, having corresponding recitations. Note similar recitations in claims 41, 43, 45, 46 and 47.

Moreover, it is respectfully submitted that the teachings of the applied references do not disclose, nor would have suggested, such method of fabricating a semiconductor device as in the present claims, including forming the trench; thermally oxidizing a trench portion formed in the substrate and burying a buried insulating film into the trench so thermally oxidized, the insulating film also being formed on the oxidation prevention film; after burying the buried insulating film, performing an additional thermal oxidation so as to selectively oxidize the semiconductor substrate at the upper end portion of the trench, to increase the radius of curvature in the proximity of the upper end portion of the trench, and substantially without oxidizing other portions of the semiconductor substrate lining the trench; and after burying the buried insulating film, removing the insulating film on the oxidation prevention film on the circuit formation surface and on the buried insulating film over the trench. See claim 54.

In general, and as will be discussed further infra, it is respectfully submitted that the applied references do not disclose, nor would have suggested, and in fact would have taught away from, the method of fabricating a semiconductor device as in the present claims, including the thermal oxidation of the trench and then, after burying insulation material in the trench, performing additional, selective thermal oxidation to selectively oxidize the semiconductor substrate at the upper end portion of the trench, to increase the radius of curvature at the upper end portion and substantially without oxidizing other portions of the substrate lining the trench.

Furthermore, it is respectfully submitted that these references would have neither taught nor would have suggested the presently claimed method, having features as discussed previously, and; moreover, wherein the trench is provided by a two-step procedure, a first step wherein a shallow trench having a radius of curvature at corners thereof is formed, and thereafter a trench having a predetermined depth to the shallow trench is formed. Note, e.g., claims 2, 5, 43 and 54.

Moreover, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such a method of fabricating a semiconductor device as in the present claims, having features as discussed in connection with the independent claims, and additionally wherein the chemically mechanically polished surface is formed over the circuit formation surface and over the trench, and wherein in the selective thermal oxidation, the semiconductor substrate having the chemically mechanically polished surface formed over the circuit formation region and over the trench is selectively thermally oxidized. See claims 56-66.

In addition, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested the other aspects of the present invention as in the remaining claims, having features as discussed previously, and further including (but not limited to) wherein the step for forming shallow trenches is carried out by isotropic etching and the step for forming trenches having a predetermined depth is carried out by anisotropic etching (see claims 3 and 6); and/or wherein providing the curvature includes forming bird's beaks at the upper end portion

of the trench (note claim 12); and/or wherein providing the curvature is performed such that an angle between the circuit formation surface of the semiconductor substrate and a side surface of the semiconductor substrate forming the trench is within a range of 90° and 180° (see claim 13); and/or material of the buried insulating film and the technique for formation thereof as in claims 18-38; and/or wherein the oxidation prevention film is removed after performing the additional thermal oxidation (see, e.g., claims 39, 42, 44 and 48, as well as claims 49-53).

The invention as presently claimed in the above-identified application is directed to a method of manufacturing a semiconductor substrate, or semiconductor device, having a trench isolation structure. A process forming a so-called "trench isolation structure", which forms trenches extending into the substrate from the substrate surface and then selectively oxidizes the trenches to form a thermal oxide film, has been employed to form insulating/isolation structure of semiconductor devices, as described in the paragraph bridging pages 1 and 2 of Applicants' specification.

In the trench isolation structure, end portions (corner points) essentially exist near the trench upper end portion of the semiconductor substrate. Stress concentration fields (both mechanical stress and electrical stress) are formed near these end portions. Because such stress concentration fields are formed, the shape of the substrate, particularly near the trench upper end portion, is oxidized in some cases into a pointed shape having an acute angle, as shown by the structure represented by reference character 4 in Fig. 1C of Applicants' original disclosure. If such an acute angle portion 4 remains on the semiconductor surface, however, concentration of

electric field occurs at this acute angle portion during circuit operation and deteriorates the breakdown voltage characteristics of, e.g., transistors, capacitors, etc., formed using such substrate. Moreover, mechanical stress fields, which are disadvantageous, are also formed. See the paragraph bridging pages 3 and 4 of Applicants' specification.

Additional problems can arise where trenches are filled with a burying material, such as buried insulating material of chemically vapor deposited silicon oxide, for example. If additional thermal oxidation is performed after burying the buried insulating film, this additional thermal oxidation oxidizing the semiconductor substrate lining the trench, volume expansion caused by the thermal oxidation after filling the trench causes a compressing stress of the semiconductor substrate due to the volume expansion of the filled trench, such stress deteriorating characteristics of electrical devices formed using the substrate.

Against this background, Applicants provide a process wherein trench isolation can be utilized, without causing deterioration of breakdown voltage characteristics of devices such as transistors and capacitors formed using the substrate with the trench isolation structure, while providing semiconductor devices having a high reliability, and wherein compressing stresses on the semiconductor substrate lining the trench are avoided. Moreover, Applicants fabricate the structure using a relatively simple technique.

Applicants have found that the desired structure, avoiding problems as discussed in the foregoing, can be achieved by preventing a substrate shape in the

proximity of the upper end portion of the device isolation trench from becoming an acute angle; and, by the present invention, provide simple techniques for preventing such acute angle, while avoiding other problems arising due to stresses in the semiconductor substrate adjacent the trenches. Specifically, according to an aspect of the present invention, Applicants provide procedures which can easily and effectively provide a curvature (increased curvature) only of an upper end portion of the trench, by a selective thermal oxidation which selectively oxidizes only the upper end portion. For example, and specifically, according to aspects of the present invention, after an initial thermal oxidation providing curvature at the upper end portion of the trench, and thereafter burying the buried insulating film, this insulating film also being formed on an oxidation prevention film on the semiconductor substrate, this insulating film on the oxidation prevention film is removed, e.g., by chemical mechanical polishing, leaving the insulating film buried in the trench and, e.g., the structure having a chemically mechanically polished surface on the insulating film over the trench and on the oxidation prevention film over a circuit formation surface of the semiconductor substrate; and the upper end portion of the trench is selectively thermally oxidized while lower portions of the trench (in particular, the semiconductor substrate lining the trench extending from the upper end portion) are substantially not oxidized, whereby the semiconductor substrate can be thermally oxidized (selectively) at only the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench.

Removal of the insulating film from the oxidation prevention film over the circuit formation surface and over the trench, prior to the additional, selective thermal oxidation, can, for example, uncover upper end portions of the trench, facilitating selective thermal oxidation of the upper end portions. As the chemically mechanically polished surface over the oxidation prevention film on the circuit formation surface and over the trench is subjected to the selective thermal oxidation, the insulating film surface over the trench is sufficiently higher than the surface of the substrate such that selective thermal oxidation as in the present claims can easily be achieved; compare with the structure that is thermally oxidized that is shown in Fig. 7 of Mehta, et al., wherein the burying material surface is relatively close to the surface of the substrate.

Moreover, after burying the buried insulating film and removal of this insulating film from the oxidation prevention film on the substrate, an upper end portion of the trench can be provided with curvature (increased curvature), which prevents the acute angle. Thus, prevention of the acute angle can be achieved, for example, by thermal oxidation of substantially only the upper end portion of the trench, after the initial oxidation and burying, e.g., by forming bird's beaks only at the upper end portion of the trench.

It is emphasized that according to the present invention, two thermal oxidation steps are performed with, e.g., an oxidation resistant film in place, a first prior to burying the trench and a second after burying the trench, the second thermal oxidation being performed as a selective thermal oxidation that oxidizes only upper end portions of the trench. With the two thermal oxidations, particularly wherein the second

(additional), selective thermal oxidation thermally oxidizes only upper end portions of the trenches, the aforementioned acute angle can be avoided, while also avoiding undesirable compressing stresses on the semiconductor substrate lining the trenches.

Thus, according to the present invention as claimed in the above-identified application, there are two thermal oxidation steps, with the trench being buried between the first and second thermal oxidation steps. In the first thermal oxidation step, an oxidation film is formed on the surface of the trench, with a curvature to some degree being formed at the upper end of the trench. Since this first thermal oxidation film is formed before the trench is buried, even by carrying out thermal oxidation with volume expansion by oxidizing the trench, since the trench is not filled a compressing stress does not form along the substrate lining the trench, so that deterioration of electrical properties, due to such compressing stress, is avoided.

In the second thermal oxidation step, the additional thermal oxidation is carried out in the condition that an insulating film is buried in the trench; accordingly, only the upper end portions of the trench are selectively thermally oxidized, without thermally oxidizing other portions of the semiconductor substrate lining the trench. Thus, since, e.g., bottom portions and bottom side portions of the trench are not thermally oxidized, deterioration of the properties due to compressing stress can be avoided. Furthermore, since upper end portions of the trench are selectively thermally oxidized, a sufficient curvature is formed at upper end portions of the trench, avoiding the sharp angle thereat and adverse effects thereof.

Moreover, according to additional aspects of the present invention, and as discussed previously, by performing selective thermal oxidation of the chemically mechanically polished surface formed on the oxidation prevention film over the circuit formation region and over the trench, a desired surface for performing the selective thermal oxidation is provided. That is, as seen in, e.g., Fig. 6K of Applicants' original disclosure, the buried material overlying the trench extends above the surface of the semiconductor substrate, thereby providing a more effective structure for the selective thermal oxidation. Compare with, for example, Fig. 7 of Mehta, et al., wherein the structure subjected to the second oxidation has a recessed upper surface over the trench relative to the surface of the oxidation resistant film 18. It is respectfully submitted that with the structure being oxidized as shown in Fig. 7 of Mehta, et al., having surface 66 relatively close to the substrate, stress occurs due to oxidation of the substrate lining the trench, and/or a gap may occur at the upper end due to concentration of stress. Such problems, which can arise in connection with Mehta, et al., would not effectively achieve the results and advantages according to the present invention.

To emphasize, according to various aspects of the present invention including selective oxidation of only upper end portions of the trench in the selective oxidation step, various advantages are achieved, including avoidance of an increase of stress due to compressing stress along the substrate lining the trench, and narrowing of the element formation region due to enlargement of bird's beak at the upper end portions of the trench. According to the present invention, sufficient curvature is achieved to

avoid decrease in electrical properties caused by the sharp angle at the upper end portions of the trench, while disadvantageous narrowing of the element formation region due to undue enlargement of the bird's beak at the upper end portions of the trench can be avoided.

Applicants' original disclosure clearly sets forth advantages according to the present invention, having the two thermal oxidation steps, the oxidation resistant film formation, and etching back the burying insulating film. That is, as is clear according to the specification of the above-identified application, since the buried insulating film 9 (see, e.g., Figs. 6G and 6H of Applicants' original disclosure) has already been formed inside the trench of the silicon substrate 1, especially wherein the insulating film 9 has been removed from on the oxidation prevention film (e.g., at the upper end portion of the trench), oxidation proceeds from near the trench upper end portion 12, and the inside of the trench is hardly oxidized. That is, a longer time is necessary for oxidation seeds to diffuse inside the buried insulating film 9 before reaching the silicon substrate 1 at lower portions of the trench, than when the silicon substrate is directly oxidized. Therefore, oxidation hardly proceeds substantially near the bottom of the trench.

On the other hand, a weak boundary layer of the coupling portion deposited by chemical vapor deposition or sputtering to the trench side walls and the upper surface of the trench exists at the trench upper end portion 12, and oxidation seeds can diffuse at a relatively high rate along this weak boundary layer, and especially where the insulating film has been removed from on the oxidation prevention film. As a result,

oxidation seeds are supplied to the trench upper end portion 12 within a short time, so that only the portions in the proximity of the trench upper end portion 12 are oxidized preferentially and the formation of the radius of curvature at the trench upper end portion 12 is promoted.

Note, for example, the paragraph bridging pages 24 and 25 of Applicants' specification, referring, inter alia, to the first embodiment. See also the paragraph bridging pages 14 and 15 of Applicants' specification, in connection with the first embodiment. See also page 26 of Applicants' specification, in connection with the third embodiment.

Mehta, et al. discloses a fabrication method for creating wide and narrow isolation regions. The method includes steps of selectively providing an etch resist layer over the wide spacing and exclusive of the narrow spacing, etching the semiconductor structure to increase the depth of the narrow spacing to form a narrow trench, growing an oxide liner in the narrow trench and in the wide spacing, providing a trench fill oxide layer over the nitride layer and the oxide liner in the wide spacing and in the narrow trench, and field oxidizing the wide spacing and the narrow trench. See column 2, lines 4-12. Note also column 2, lines 22-32 and 51-53. Note further column 3, lines 5-7. In a specific embodiment shown in Figs. 5 and 6, this patent discloses that after layer 60 is subjected to an oxide etch, structure 12 is subjected to thermal oxidation to grow the oxide in spacing 44 and 46 by local oxidation of silicon techniques. The growing of layers 60 in spacings 44 and 46 provides a deeper insulative region in both regions 24 and 28 of structure 12. Once subjected to thermal

oxidation, the insulative material in regions 24 and 28 grows in a direction toward nitride layer 18 and base 14; and, therefore, providing conventional LOCOS operation on spacings 44 and 46 creates effective isolation regions 24 and 28 for structure 12. See column 5, lines 55-65.

Of particular relevance is the following description set forth in Mehta, et al., at column 5, lines 58-62 (that is, the portion of Mehta, et al. immediately subsequent to that portion of Mehta, et al. referred to by the Examiner in the second full paragraph on page 23 of the Office Action mailed June 1, 2004):

> "The growing of layers 60 in spacings 44 and 46 provides a deeper insulative region in both regions 24 and 28 of structure 12. When subjected to thermal oxidation, the insulative material in regions 24 and 28 grows in a direction towards nitride layer 18 and base 14". (Emphasis added).

It is emphasized that according to the teachings of Mehta, et al., in the thermal oxidation after layer 60 has been subjected to oxide etch, layer 60 grows providing a deeper insulative region in both regions 24 and 28, the insulative material in regions 24 and 28 growing, inter alia, in a direction toward base 14. It is respectfully submitted that this disclosure in Mehta, et al., with respect to growth of the thermal oxide towards the base 14, would have neither disclosed nor would have suggested, and in fact would have taught away from, the presently claimed invention, including wherein the selective thermal oxidation is performed to oxidize only a portion of the substrate at the upper end portion of the trench, and not substantially at other portions of the substrate lining the trench, to provide an increase in curvature of the upper end portion of the trench

substantially without oxidizing other portions of the semiconductor substrate lining the trench.

It is respectfully submitted that Mehta, et al. has an entirely different purpose from that of the present invention. That is, Mehta, et al. is concerned with providing a narrow trench isolation region and a wide LOCOS isolation region, for eliminating or reducing dishing due to different widths of trench isolation regions. In contrast, the present invention is directed to avoiding deterioration of electrical properties due to sharp angles and/or stresses arising with trench isolation, including stresses caused by growth of thermal oxide along the trench lines after filling the trench. Particularly noting the purpose of Mehta, et al., including the purpose of growing the insulative material in a direction toward the base (that is, along the trench liner, after filling the trench), as described in column 5, lines 55-65, this patent would have taught away from the present invention.

The contention by the Examiner that Mehta, et al. discloses performing oxidation so as to oxidize only a portion of the semiconductor substrate at the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench, is respectfully traversed. Again, it is emphasized that Mehta, et al. specifically discloses thermal oxidation to grow the insulative material in regions 24 and 28 in a direction towards base 14, and provides a deeper insulative region. Such disclosure would have taught away from, and clearly would have neither disclosed nor would have suggested, performing oxidation so as to oxidize only a portion of the substrate at the upper end portion of the trench, as in the present invention.

Applicants respectfully traverse the conclusion by the Examiner on page 23 of the Office Action mailed June 1, 2004, that Mehta, et al. teaches selective thermal oxidation that only oxidizes the upper end portion of trench 44 and not other portions of the semiconductor substrate lining the trench. Again, attention is respectfully directed to the above-quoted description from Mehta, et al., set forth at column 5, lines 58-62 of Mehta, et al. Clearly, Mehta, et al. describes that the isolative material grows in a direction toward, inter alia, base 14. Clearly, Mehta, et al. would have taught away from the presently claimed invention, including wherein the selective thermal oxidation is performed substantially without oxidizing the other portions of the semiconductor substrate lining the trench, and advantages thereof as discussed in the foregoing.

The contention by the Examiner on page 23 of the Office Action mailed June 1, 2004, that Applicants fail to identify which portions of Mehta, et al. would have taught away from the present invention as claimed, is noted. As is clear from the foregoing, as well as from, for example, pages 38 and 39 of the Submission (Amendment) filed November 3, 2003, the disclosure in Mehta, et al., of the insulative material growing in the direction toward base 14, would have taught away from the presently claimed method, including the selective thermal oxidation substantially without oxidizing portions of the substrate lining the trenches, and advantages thereof as discussed in the foregoing (that is, for example, avoidance of stress and degraded characteristics due thereto).

It is respectfully submitted that the additional teachings of Takahashi would not have rectified the deficiencies of Mehta, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Takahashi discloses a method of fabricating a semiconductor device in which device isolation is made by a trench formed in a semiconductor substrate, the method including a first step of forming a device-isolating trench with a taper at an upper portion thereof, in a semiconductor substrate; and a second step of forming an oxide film on an inner wall of the trench and a surface of the semiconductor substrate near the trench. See the paragraph bridging columns 1 and 2 of Takahashi. Note also column 2, lines 53-58; column 3, lines 7-12, 17-25, 35-39 and 41-46; and column 4, lines 39-54.

Even assuming, arguendo, that the teachings of Takahashi were properly combinable with the teachings of Mehta, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including the selective thermal oxidation which thermally oxidizes only a portion of the substrate, at the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench, so as to increase a curvature of the upper end portion of the trench substantially without oxidizing the other portions of the semiconductor substrate lining the trench, and advantages thereof as discussed in the foregoing; and/or the other aspects of the present invention as discussed in the foregoing, and advantages thereof.

The additional contention by the Examiner on page 23 of the Office Action mailed June 1, 2004, that Mehta, et al. teaches that the thermal oxidation is performed after the chemically mechanically polished surface 66 has been formed, is noted. It is respectfully submitted, however, as described at column 5, lines 46-54 of Mehta, et al., the top surface 66 of layer 60 in spacing 44 and the top surface 68 of layer 60 in spacing 46 are further etched by an oxide etch selective to nitride, such as a wet etching technique, RIE technique, plasma etch or other etching process. In view thereof, it is respectfully submitted that Mehta, et al. would have neither taught nor would have suggested, and in fact would have taught away from, selective thermal oxidation of the substrate having the specified chemically mechanically polished surface, as in the present claims, and in particular claims 56-66; and/or, more generally, wherein selective thermal oxidation of the semiconductor substrate is performed after having formed the chemically mechanically polished surface as in the present claims.

It is respectfully submitted that the additional teachings of Otsu would not have rectified the deficiencies of the teachings of Mehta, et al. and Takahashi, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Otsu discloses a manufacturing method of a metal-insulator-semiconductor device using trench isolation techniques, in which a gate electrode is formed to cover the upper portion of an element or device forming region which is isolated by a trench. The method is described generally in column 2, lines 43-55. See also the paragraph

bridging columns 2 and 3 of this patent. Note further column 4, lines 3-18 and 39-58; and column 5, lines 5-16.

Even assuming, arguendo, that the teachings of Otsu were properly combinable with the teachings of Mehta, et al. and of Takahashi, such combined teachings would have neither disclosed nor would have suggested the presently claimed method, including the chemically mechanically polished surface formed and the selective thermal oxidation so as to thermally oxidize only a portion of the semiconductor substrate, at the upper end portion of the trench, and not substantially at other portions of the semiconductor substrate lining the trench, and advantages of the present invention as discussed previously.

Applicants respectfully traverse the contention by the Examiner that the additional thermal oxidation of Mehta, et al. "only" oxidizes the upper end portion of trench (44). It is respectfully submitted that this is directly contrary to the express and specific description in Mehta, et al. of the growing of layers 60 to provide a deeper insulative region, wherein, when subjected to thermal oxidation, the insulative material in regions 24 and 28 grow in a direction, inter alia, towards base 14. Taking the teachings of Mehta, et al. as a whole, as required under 35 USC §102 and 35 USC §103, it is respectfully submitted that this reference teaches away from the selective oxidation as in various of the present claims.

The contention by the Examiner that Applicants fail to identify what portions of the reference would have taught away from the present invention as claimed, is noted. Applicants clearly have pointed out that Mehta, et al. would have taught away from,

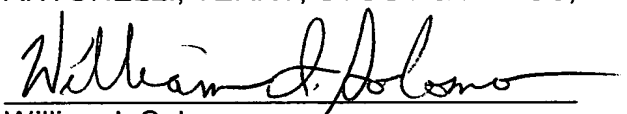
inter alia, the selective additional thermal oxidation which oxidizes only a portion of the substrate at the upper end portions of the trenches, and not substantially at other portions of the semiconductor substrate lining the trenches. It is respectfully submitted that the Examiner is improperly ignoring express and specific teachings of Mehta, et al., contrary to requirements of 35 USC §103, in coming to a conclusion concerning obviousness.

In view of the foregoing comments and amendments, entry of the present amendments, and reconsideration and allowance of all claims remaining in the application, are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (500.36904X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



William I. Solomon
Registration No. 28,565

1300 North Seventeenth Street
Suite 1800
Arlington, VA 22209
Tel.: 703-312-6600
Fax.: 703-312-6666
WIS/sjg